



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Edgar R. Zuniga-Ortiz, et al.**
Serial No.: **10/001,302**
Filed: **11/01/2001**
For: **Bumpless Wafer Scale Device And Board Assembly**

Docket No.: **TI-33535**

Examiner: **Clark, Sheila**

Art Unit: **2815**

Conf. No.: **2463**

RECEIVED
FEB 27 2003
TECHNICAL CENTER 2800

ELECTION

Assistant Commissioner For Patents
Washington, D.C. 20231

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that on this day the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231.

Elizabeth Austin

Date

2/18/2003

This election is offered in response to the Examiner's restriction requirement dated January 28, 2003. The Examiner has required restriction to one of the groups of: Group I, Claims 1-25 or Group II, Claims 26-32.

Applicant hereby elects to pursue Group I, Claims 1-25 without traversing the Examiner's restriction requirement.

Respectfully submitted,

Michael K. Skrehot
Patent Attorney
Reg. No. 36,682

Texas Instruments Incorporated
P. O. Box 655474, M. S. 219
Dallas, Texas 75265
(972) 917-5653